LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (Currently Amended) A system for providing a temporarily modified output, comprising:

a waveform control that provides a control output that temporarily adjusts to an intermediate level during a transition between normal high and low levels during a first operating mode, the waveform control provides the control output to transition periodically between the high and low levels during a second operating mode;

a delay network that controls the waveform control to provide the output at the intermediate level for a duration during the first operating mode; ~~and~~

a driver that provides an output signal based on the control output provided by the waveform control, the output signal transitions between associated high and low levels during the second operating mode, and transitions to an intermediate level for the duration during the first operating mode; and

the waveform control further comprising at least one component coupled to temporarily diode connect a transistor device of the driver, by providing each of a control input node and a second node of the transistor device with a matched voltage, to enable the driver to provide the output signal at the intermediate level for the duration of the first operating mode.

Claim 3 (Canceled)

4. (Currently Amended) The system of claim ~~3~~, 1, the waveform control further comprising a logic network that controls operation of the at least one component based at least in part on a delayed signal provided by the delay network.

5. (Original) The system of claim 2, the driver further comprising at least first and second inputs, the control output provided by the waveform control further comprising a

first control output that is provided to the first input of the driver and a second control output that is provided to the second input of the driver.

6. (Original) The system of claim 5, the output signal self-biases to the intermediate level during the first operating mode based on relative characteristics of at least some devices that form the driver.

7. (Previously Presented) The system of claim 6, the devices that form the driver comprising at least one transistor of a first type associated with the first input of the driver and at least one transistor of a second type associated with the second input of the driver, the relative characteristics corresponding to the relative strengths of the at least one transistor of the first type and the at least one transistor of the second type.

8. (Currently Amended) A system for providing a temporarily modified output, comprising:

a waveform control that provides a control output that temporarily adjusts to an intermediate level during a transition between normal high and low levels during a first operating mode, the waveform control provides the control output to transition periodically between the high and low levels during a second operating mode;

a delay network that controls the waveform control to provide the output at the intermediate level for a duration during the first operating mode;

a driver that provides an output signal based on the control output provided by the waveform control, the output signal transitions between associated high and low levels during the second operating mode, and transitions to an intermediate level for the duration during the first operating mode, the driver further comprising at least first and second inputs, the control output provided by the waveform control further comprising a first control output that is provided to the first input of the driver and a second control output that is provided to the second input of the driver; and

~~The system of claim 5,~~ the waveform control couples the first and second inputs of the driver together except for the duration during the first operating mode, the waveform control provides the first and second control outputs to the driver at associated intermediate levels between respective normal high and low levels for the duration during the first operating mode.

9. (Original) The system of claim 8, the waveform control further comprising circuitry coupled to temporarily diode connect a device of the driver such that at least a portion of the circuitry of the waveform control and the driver component cooperate to define a circuit arrangement that causes the driver to provide the output signal at the intermediate level for the duration of the first operating mode.

10. (Original) The system of claim 2, further comprising a precharge device that charges an associated node based on the output signal provided by the driver, the precharge device partially conducts based on the intermediate level of the output signal during the first operating mode, thereby operating as a supplemental keeper to precharge the associated node.

11. (Original) The system of claim 10, the output signal biases the precharge device at the intermediate level, which self biases according to a relative strength of at least some devices that form the driver, the relative strength of the at least some devices being related to process variations in the devices in the driver.

Claims 12-13 (Cancelled)

14. (Currently Amended) An integrated circuit chip comprising:

~~A~~ a clock generator of the integrated circuit chip comprising:

a waveform control that provides a control output that temporarily adjusts to an intermediate level during a transition between normal high and low levels during a first operating mode, the waveform control provides the control output to transition periodically between the high and low levels during a second operating mode;

a delay network that controls the waveform control to provide the control output at the intermediate level for a duration during the first operating mode;

a predriver coupled to control the waveform control; and

a driver that provides an output clock signal based on the control output;

at least one associated circuit of the integrated circuit chip driven by the output clock signal provided by the driver of the clock generator;

each of the at least one associated circuits of the integrated circuit chip further comprising a precharge device that provides a charge at an associated node based on the output clock signal.

15. (Previously Presented) The integrated circuit of claim 14, each of the at least one associated circuits comprising a domino logic circuit that includes the precharge device, the first operating mode corresponds to a noise reduction mode, such that the control output at the intermediate level facilitates evaluation of the at least one circuit during the noise reduction mode.

16. (Currently Amended) A clock generator comprising:

a driver that provides an output clock signal based on at least one control signal; and

a waveform controller that provides the at least one control signal having a first waveform characteristic during a first operating mode to control the driver to provide the output clock signal having normally high and low levels, the waveform controller provides the at least one control signal having a second waveform characteristic during a second operating mode to control the driver to temporarily transition the output clock signal directly from one of the normally high and low levels to an intermediate level between the normally high and low levels and then transition the output clock signal directly from the intermediate level to the other of the normally high and low levels; and

at least one device that temporarily diode connects a transistor device of the driver, by providing a control input node and a second node of the transistor device with a matched voltage, to provide a diode-connected transistor device that enables the driver to provide the output clock signal at the intermediate level during the second operating mode.

Claim 17 (Canceled)

18. (Currently Amended) The clock generator of claim ~~17,~~ 16, further comprising a network coupled to control the at least one device to implement the temporary diode connection based at least in part on a feedback signal that varies according to a delay implemented by the waveform controller.

19. (Original) The clock generator of claim 16, the driver further comprising at least first and second inputs, the at least one control signal provided by the waveform controller further comprising a first control signal that is provided to the first input of the driver and a second control signal that is provided to the second input of the driver, the first and second control signals having substantially identical waveforms during the first operating mode so that the output clock signal transitions between the normally high and low levels, the waveform controller provides the first and second control signals to the driver as waveforms having respective intermediate levels so that the driver temporarily provides the output clock signal at the intermediate level during the second operating mode.

20. (Original) The clock generator of claim 19, the driver further comprising at least one transistor of a first type associated with the first input of the driver and at least one transistor of a second type associated with the second input of the driver, the relative characteristics corresponding to the relative strengths of the at least one transistor of the first type and the at least transistor of the second type.

21. (Previously Presented) The clock generator of claim 16, the waveform controller further comprising circuitry and the driver further comprising circuitry, at least a portion of the waveform controller circuitry cooperating with at least a portion of the driver circuitry to form a voltage divider during the second operating mode in which a node of the voltage divider provides the output clock signal at the intermediate level during the second operating mode.

22 (Currently Amended) The clock generator of claim 21, ~~the circuitry of the waveform controller temporarily diode connects at least one device of the driver~~ the diode-connected transistor device of the driver forms part of the voltage divider.

23. (Original) The clock generator of claim 16, the output clock signal self-biases to the intermediate level during the second operating mode based on relative characteristics of at least some components that form the driver.

24. (Original) The clock generator of claim 16, further comprising a delay network associated with the waveform controller to control a duration for which the output clock signal is at the intermediate level during the second operating mode.

25. (Previously Presented) A clock generator comprising:

a driver that provides an output clock signal based on at least one control signal;

a waveform controller that provides the at least one control signal having a first waveform characteristic during a first operating mode to control the driver to provide the output clock signal having normally high and low levels, the waveform controller provides the at least one control signal having a second waveform characteristic during a second operating mode to control the driver to temporarily transition the output clock signal from one of the normally high and low levels to an intermediate level between the normally high and low levels and then transition the output clock signal from the intermediate level to the other of the normally high and low levels; and

a precharge device that charges an associated node based on the output clock signal provided by the driver, the precharge device partially conducts according to the intermediate level of the output clock signal during the second operating mode, thereby operating as a supplemental keeper to precharge the associated node during the second operating mode.

26. (Currently Amended) An integrated circuit chip comprising:

the clock generator of claim 16; and

at least one circuit driven by the output clock signal from the driver of the clock generator.

27. (Currently Amended) The integrated circuit chip of claim 26, the at least one circuit further comprising a precharge device that provides a charge at an associated node based on the output clock signal, the second operating mode corresponds to a noise reduction mode in which the precharge device partially conducts in response to the driver providing the output clock signal at the intermediate level, whereby evaluation of the at least one circuit during the noise reduction mode is facilitated.

Claims 28-29 (Cancelled)

30. (Currently Amended) A system for providing a temporary reduced output, comprising:

means for providing a control signal that periodically transitions between normally high and low levels during a normal operating mode; and

means for, during an operating mode that is different from the normal operating mode, controlling the means for providing to temporarily modify the control signal to an intermediate level during a transition of the control signal between the normally high and low levels, the intermediate level being between the normally high and low levels during the operating mode that is different from the normal operating mode;

means for providing a clock signal for driving associated circuitry based on the control signal; ~~and~~

means for providing the clock signal at an intermediate level that self-biases between normal high and low levels according to process variations in the system, and

means for supplying a charge to a node of associated circuitry based on the clock signal, the means for supplying provides a supplemental charge to the node for a duration that is commensurate with a duration that the clock signal is provided at the intermediate level, whereby evaluation of the associated circuitry is facilitated.

Claim 31 (Canceled)

32. (Previously Presented) The system of claim 30, further comprising means for controlling a duration for which the control signal is provided at the intermediate level.

Claims 33-34 (Cancelled)